**LAB MANUAL NO 19**

**ALU**

module andd(

input [31:0] a,

input [31:0] b,

output [31:0] C

);

assign C=a&b;

endmodule

module orr(

input [31:0] a,

input [31:0] b,

output [31:0] C

);

assign C=a|b;

endmodule

module thirtytwo\_bitsub(

input [31:0]a,

input [31:0]d,

output [31:0]s

);

reg cin1=1'b1;

wire Carry1,Carry2,Carry3,Carry4,Carry5,Carry6,Carry7,Carry8,Carry9,Carry10,Carry11,Carry12,Carry13,Carry14,Carry15,Carry16,Carry17,Carry18,Carry19,Carry20,

Carry21,Carry22,Carry23,Carry24,Carry25,Carry26,Carry27,Carry28,Carry29,Carry30,Carry31;

wire [31:0]b;

neg neg1(d,b);

fulladderr fa\_1( a[0], b[0], cin1, s[0], Carry1);

fulladderr fa\_2( a[1], b[1], Carry1, s[1], Carry2);

fulladderr fa\_3( a[2], b[2], Carry2, s[2], Carry3);

fulladderr fa\_4( a[3], b[3], Carry3, s[3], Carry4);

fulladderr fa\_5( a[4], b[4], Carry4, s[4], Carry5);

fulladderr fa\_6( a[5], b[5], Carry5, s[5], Carry6);

fulladderr fa\_7( a[6], b[6], Carry6, s[6], Carry7);

fulladderr fa\_8( a[7], b[7], Carry7, s[7], Carry8);

fulladderr fa\_9( a[8], b[8], Carry8, s[8], Carry9);

fulladderr fa\_10( a[9], b[9], Carry9, s[9], Carry10);

fulladderr fa\_11( a[10], b[10], Carry10, s[10], Carry11);

fulladderr fa\_12( a[11], b[11], Carry11, s[11], Carry12);

fulladderr fa\_13( a[12], b[12], Carry12, s[12], Carry13);

fulladderr fa\_14( a[13], b[13], Carry13, s[13], Carry14);

fulladderr fa\_15( a[14], b[14], Carry14, s[14], Carry15);

fulladderr fa\_16( a[15], b[15], Carry15, s[15], Carry16);

fulladderr fa\_17( a[16], b[16], Carry16, s[16], Carry17);

fulladderr fa\_18( a[17], b[17], Carry17, s[17], Carry18);

fulladderr fa\_19( a[18], b[18], Carry18, s[18], Carry19);

fulladderr fa\_20( a[19], b[19], Carry19, s[19], Carry20);

fulladderr fa\_21( a[20], b[20], Carry20, s[20], Carry21);

fulladderr fa\_22( a[21], b[21], Carry21, s[21], Carry22);

fulladderr fa\_23( a[22], b[22], Carry22, s[22], Carry23);

fulladderr fa\_24( a[23], b[23], Carry23, s[23], Carry24);

fulladderr fa\_25( a[24], b[24], Carry24, s[24], Carry25);

fulladderr fa\_26( a[25], b[25], Carry25, s[25], Carry26);

fulladderr fa\_27( a[26], b[26], Carry26, s[26], Carry27);

fulladderr fa\_28( a[27], b[27], Carry27, s[27], Carry28);

fulladderr fa\_29( a[28], b[28], Carry28, s[28], Carry29);

fulladderr fa\_30( a[29], b[29], Carry29, s[29], Carry30);

fulladderr fa\_31( a[30], b[30], Carry30, s[30], Carry31);

fulladderr fa\_32( a[31], b[31], Carry31, s[31], Carry32);

endmodule

module neg(

input [31:0] g,

output [31:0] h

);

assign h=~g;

endmodule

module fulladderr(

input wire a,

input wire b,

input wire cin,

output Sum,

output Carry

);

reg T1,T2;

assign Carry=(a&b)|(b&cin)|(a&cin);//Data flow modelling

always@(a or b or cin) //Behavioural Modelling

begin

T1=a^b;

T2=cin;

end

xor(Sum,T1,T2);// Structural modelling

endmodule

module thirtytwo\_bitadder(

input [31:0]a,

input [31:0]b,

input cin1,

output [31:0]s,

output Carry32

);

wire Carry1,Carry2,Carry3,Carry4,Carry5,Carry6,Carry7,Carry8,Carry9,Carry10,Carry11,Carry12,Carry13,Carry14,Carry15,Carry16,Carry17,Carry18,Carry19,Carry20,

Carry21,Carry22,Carry23,Carry24,Carry25,Carry26,Carry27,Carry28,Carry29,Carry30,Carry31;

fulladder fa\_1( a[0], b[0], cin1, s[0], Carry1);

fulladder fa\_2( a[1], b[1], Carry1, s[1], Carry2);

fulladder fa\_3( a[2], b[2], Carry2, s[2], Carry3);

fulladder fa\_4( a[3], b[3], Carry3, s[3], Carry4);

fulladder fa\_5( a[4], b[4], Carry4, s[4], Carry5);

fulladder fa\_6( a[5], b[5], Carry5, s[5], Carry6);

fulladder fa\_7( a[6], b[6], Carry6, s[6], Carry7);

fulladder fa\_8( a[7], b[7], Carry7, s[7], Carry8);

fulladder fa\_9( a[8], b[8], Carry8, s[8], Carry9);

fulladder fa\_10( a[9], b[9], Carry9, s[9], Carry10);

fulladder fa\_11( a[10], b[10], Carry10, s[10], Carry11);

fulladder fa\_12( a[11], b[11], Carry11, s[11], Carry12);

fulladder fa\_13( a[12], b[12], Carry12, s[12], Carry13);

fulladder fa\_14( a[13], b[13], Carry13, s[13], Carry14);

fulladder fa\_15( a[14], b[14], Carry14, s[14], Carry15);

fulladder fa\_16( a[15], b[15], Carry15, s[15], Carry16);

fulladder fa\_17( a[16], b[16], Carry16, s[16], Carry17);

fulladder fa\_18( a[17], b[17], Carry17, s[17], Carry18);

fulladder fa\_19( a[18], b[18], Carry18, s[18], Carry19);

fulladder fa\_20( a[19], b[19], Carry19, s[19], Carry20);

fulladder fa\_21( a[20], b[20], Carry20, s[20], Carry21);

fulladder fa\_22( a[21], b[21], Carry21, s[21], Carry22);

fulladder fa\_23( a[22], b[22], Carry22, s[22], Carry23);

fulladder fa\_24( a[23], b[23], Carry23, s[23], Carry24);

fulladder fa\_25( a[24], b[24], Carry24, s[24], Carry25);

fulladder fa\_26( a[25], b[25], Carry25, s[25], Carry26);

fulladder fa\_27( a[26], b[26], Carry26, s[26], Carry27);

fulladder fa\_28( a[27], b[27], Carry27, s[27], Carry28);

fulladder fa\_29( a[28], b[28], Carry28, s[28], Carry29);

fulladder fa\_30( a[29], b[29], Carry29, s[29], Carry30);

fulladder fa\_31( a[30], b[30], Carry30, s[30], Carry31);

fulladder fa\_32( a[31], b[31], Carry31, s[31], Carry32);

endmodule

module fulladder(

input wire a,

input wire b,

input wire cin,

output Sum,

output Carry

);

reg T1,T2;

assign Carry=(a&b)|(b&cin)|(a&cin);//Data flow modelling

always@(a or b or cin) //Behavioural Modelling

begin

T1=a^b;

T2=cin;

end

xor(Sum,T1,T2);// Structural modelling

endmodule

module fourmuxx(

input [1:0] op,

input [31:0]a,

input [31:0]b,

output reg [31:0]z

);

wire [31:0]C1,C2,s;

andd andd1(a,b,C1);

orr orr1(a,b,C2);

thirtytwo\_bitsub thirtytwo\_bitsub1(a,b,s);

always@(op,a,b,C1,C2,s)

begin

case(op)

0:z=C1;

1:z=C2;

2:z=s;

3:z=1'b0;

endcase

end

endmodule

Testbench:

module alu\_tb;

// Inputs

reg [1:0] op;

reg [31:0] a;

reg [31:0] b;

// Outputs

wire [31:0] z;

// Instantiate the Unit Under Test (UUT)

fourmuxx uut (

.op(op),

.a(a),

.b(b),

.z(z)

);

initial begin

// Initialize Inputs

op = 0;

a = 0;

b = 0;

// Wait 100 ns for global reset to finish

#100;

// Add stimulus here

op=2'b11;

a=32'b11001100110011001001100110011001;

b=32'b10011001100110011100110011001100;

#100;

end

endmodule

SYNTHESIS REPORT:

Release 12.1 - xst M.53d (nt)

Copyright (c) 1995-2010 Xilinx, Inc. All rights reserved.

--> Parameter TMPDIR set to xst/projnav.tmp

Total REAL time to Xst completion: 0.00 secs

Total CPU time to Xst completion: 0.40 secs

--> Parameter xsthdpdir set to xst

Total REAL time to Xst completion: 0.00 secs

Total CPU time to Xst completion: 0.40 secs

--> Reading design: fourmuxx.prj

TABLE OF CONTENTS

1) Synthesis Options Summary

2) HDL Compilation

3) Design Hierarchy Analysis

4) HDL Analysis

5) HDL Synthesis

5.1) HDL Synthesis Report

6) Advanced HDL Synthesis

6.1) Advanced HDL Synthesis Report

7) Low Level Synthesis

8) Partition Report

9) Final Report

9.1) Device utilization summary

9.2) Partition Resource Summary

9.3) TIMING REPORT

=========================================================================

\* Synthesis Options Summary \*

=========================================================================

---- Source Parameters

Input File Name : "fourmuxx.prj"

Input Format : mixed

Ignore Synthesis Constraint File : NO

---- Target Parameters

Output File Name : "fourmuxx"

Output Format : NGC

Target Device : xc3s200-5-pq208

---- Source Options

Top Module Name : fourmuxx

Automatic FSM Extraction : YES

FSM Encoding Algorithm : Auto

Safe Implementation : No

FSM Style : lut

RAM Extraction : Yes

RAM Style : Auto

ROM Extraction : Yes

Mux Style : Auto

Decoder Extraction : YES

Priority Encoder Extraction : YES

Shift Register Extraction : YES

Logical Shifter Extraction : YES

XOR Collapsing : YES

ROM Style : Auto

Mux Extraction : YES

Resource Sharing : YES

Asynchronous To Synchronous : NO

Multiplier Style : auto

Automatic Register Balancing : No

---- Target Options

Add IO Buffers : YES

Global Maximum Fanout : 500

Add Generic Clock Buffer(BUFG) : 8

Register Duplication : YES

Slice Packing : YES

Optimize Instantiated Primitives : NO

Use Clock Enable : Yes

Use Synchronous Set : Yes

Use Synchronous Reset : Yes

Pack IO Registers into IOBs : auto

Equivalent register Removal : YES

---- General Options

Optimization Goal : Speed

Optimization Effort : 1

Library Search Order : fourmuxx.lso

Keep Hierarchy : NO

Netlist Hierarchy : as\_optimized

RTL Output : Yes

Global Optimization : AllClockNets

Read Cores : YES

Write Timing Constraints : NO

Cross Clock Analysis : NO

Hierarchy Separator : /

Bus Delimiter : <>

Case Specifier : maintain

Slice Utilization Ratio : 100

BRAM Utilization Ratio : 100

Verilog 2001 : YES

Auto BRAM Packing : NO

Slice Utilization Ratio Delta : 5

=========================================================================

=========================================================================

\* HDL Compilation \*

=========================================================================

Compiling verilog file "neg.v" in library work

Compiling verilog file "fulladderr.v" in library work

Module <neg> compiled

Compiling verilog file "thirtytwo\_bitsub.v" in library work

Module <fulladderr> compiled

Compiling verilog file "orr.v" in library work

Module <thirtytwo\_bitsub> compiled

Compiling verilog file "fourmuxx.v" in library work

Module <orr> compiled

Module <fourmuxx> compiled

No errors in compilation

Analysis of file <"fourmuxx.prj"> succeeded.

=========================================================================

\* Design Hierarchy Analysis \*

=========================================================================

Analyzing hierarchy for module <fourmuxx> in library <work>.

Analyzing hierarchy for module <andd> in library <work>.

Analyzing hierarchy for module <orr> in library <work>.

Analyzing hierarchy for module <thirtytwo\_bitsub> in library <work>.

Analyzing hierarchy for module <neg> in library <work>.

Analyzing hierarchy for module <fulladderr> in library <work>.

=========================================================================

\* HDL Analysis \*

=========================================================================

Analyzing top module <fourmuxx>.

Module <fourmuxx> is correct for synthesis.

Analyzing module <andd> in library <work>.

Module <andd> is correct for synthesis.

Analyzing module <orr> in library <work>.

Module <orr> is correct for synthesis.

Analyzing module <thirtytwo\_bitsub> in library <work>.

Module <thirtytwo\_bitsub> is correct for synthesis.

Analyzing module <neg> in library <work>.

Module <neg> is correct for synthesis.

Analyzing module <fulladderr> in library <work>.

Module <fulladderr> is correct for synthesis.

=========================================================================

\* HDL Synthesis \*

=========================================================================

Performing bidirectional port resolution...

Synthesizing Unit <andd>.

Related source file is "andd.v".

Unit <andd> synthesized.

Synthesizing Unit <orr>.

Related source file is "orr.v".

Unit <orr> synthesized.

Synthesizing Unit <neg>.

Related source file is "neg.v".

Unit <neg> synthesized.

Synthesizing Unit <fulladderr>.

Related source file is "fulladderr.v".

Found 1-bit xor3 for signal <Sum>.

Summary:

inferred 1 Xor(s).

Unit <fulladderr> synthesized.

Synthesizing Unit <thirtytwo\_bitsub>.

Related source file is "thirtytwo\_bitsub.v".

[WARNING](WARNING:Xst:653%20-%20Signal%20%3ccin1%3e%20is%20used%20but%20never%20assigned.%20This%20sourceless%20signal%20will%20be%20automatically%20connected%20to%20value%201.?&DataKey=SolutionRecord):Xst:653 - Signal <cin1> is used but never assigned. This sourceless signal will be automatically connected to value 1.

[WARNING](WARNING:Xst:646%20-%20Signal%20%3cCarry32%3e%20is%20assigned%20but%20never%20used.%20This%20unconnected%20signal%20will%20be%20trimmed%20during%20the%20optimization%20process.?&DataKey=SolutionRecord):Xst:646 - Signal <Carry32> is assigned but never used. This unconnected signal will be trimmed during the optimization process.

Unit <thirtytwo\_bitsub> synthesized.

Synthesizing Unit <fourmuxx>.

Related source file is "fourmuxx.v".

Found 32-bit 4-to-1 multiplexer for signal <z>.

Summary:

inferred 32 Multiplexer(s).

Unit <fourmuxx> synthesized.

=========================================================================

HDL Synthesis Report

Macro Statistics

# Multiplexers : 1

32-bit 4-to-1 multiplexer : 1

# Xors : 32

1-bit xor3 : 32

=========================================================================

=========================================================================

\* Advanced HDL Synthesis \*

=========================================================================

=========================================================================

Advanced HDL Synthesis Report

Macro Statistics

# Multiplexers : 1

32-bit 4-to-1 multiplexer : 1

# Xors : 32

1-bit xor3 : 32

=========================================================================

=========================================================================

\* Low Level Synthesis \*

=========================================================================

Optimizing unit <fourmuxx> ...

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block fourmuxx, actual ratio is 3.

Final Macro Processing ...

=========================================================================

Final Register Report

Found no macro

=========================================================================

=========================================================================

\* Partition Report \*

=========================================================================

Partition Implementation Status

-------------------------------

No Partitions were found in this design.

-------------------------------

=========================================================================

\* Final Report \*

=========================================================================

Final Results

RTL Top Level Output File Name : fourmuxx.ngr

Top Level Output File Name : fourmuxx

Output Format : NGC

Optimization Goal : Speed

Keep Hierarchy : NO

Design Statistics

# IOs : 98

Cell Usage :

# BELS : 124

# LUT3 : 28

# LUT4 : 66

# MUXF5 : 30

# IO Buffers : 98

# IBUF : 66

# OBUF : 32

=========================================================================

Device utilization summary:

---------------------------

Selected Device : 3s200pq208-5

Number of Slices: 50 out of 1920 2%

Number of 4 input LUTs: 94 out of 3840 2%

Number of IOs: 98

Number of bonded IOBs: 98 out of 141 69%

---------------------------

Partition Resource Summary:

---------------------------

No Partitions were found in this design.

---------------------------

=========================================================================

TIMING REPORT

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.

FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT

GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

------------------

No clock signals found in this design

Asynchronous Control Signals Information:

----------------------------------------

No asynchronous control signals found in this design

Timing Summary:

---------------

Speed Grade: -5

Minimum period: No path found

Minimum input arrival time before clock: No path found

Maximum output required time after clock: No path found

Maximum combinational path delay: 50.138ns

Timing Detail:

--------------

All values displayed in nanoseconds (ns)

=========================================================================

Timing constraint: Default path analysis

Total number of paths / destination ports: 2144 / 32

-------------------------------------------------------------------------

Delay: 50.138ns (Levels of Logic = 33)

Source: a<1> (PAD)

Destination: z<31> (PAD)

Data Path: a<1> to z<31>

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

---------------------------------------- ------------

IBUF:I->O 3 0.715 1.066 a\_1\_IBUF (a\_1\_IBUF)

LUT4:I0->O 3 0.479 0.941 thirtytwo\_bitsub1/fa\_2/Carry1 (thirtytwo\_bitsub1/Carry2)

LUT3:I1->O 3 0.479 0.941 thirtytwo\_bitsub1/fa\_3/Carry1 (thirtytwo\_bitsub1/Carry3)

LUT3:I1->O 3 0.479 0.941 thirtytwo\_bitsub1/fa\_4/Carry1 (thirtytwo\_bitsub1/Carry4)

LUT3:I1->O 3 0.479 0.941 thirtytwo\_bitsub1/fa\_5/Carry1 (thirtytwo\_bitsub1/Carry5)

LUT3:I1->O 3 0.479 0.941 thirtytwo\_bitsub1/fa\_6/Carry1 (thirtytwo\_bitsub1/Carry6)

LUT3:I1->O 3 0.479 0.941 thirtytwo\_bitsub1/fa\_7/Carry1 (thirtytwo\_bitsub1/Carry7)

LUT3:I1->O 3 0.479 0.941 thirtytwo\_bitsub1/fa\_8/Carry1 (thirtytwo\_bitsub1/Carry8)

LUT3:I1->O 3 0.479 0.941 thirtytwo\_bitsub1/fa\_9/Carry1 (thirtytwo\_bitsub1/Carry9)

LUT3:I1->O 3 0.479 0.941 thirtytwo\_bitsub1/fa\_10/Carry1 (thirtytwo\_bitsub1/Carry10)

LUT3:I1->O 3 0.479 0.941 thirtytwo\_bitsub1/fa\_11/Carry1 (thirtytwo\_bitsub1/Carry11)

LUT3:I1->O 3 0.479 0.941 thirtytwo\_bitsub1/fa\_12/Carry1 (thirtytwo\_bitsub1/Carry12)

LUT3:I1->O 3 0.479 0.941 thirtytwo\_bitsub1/fa\_13/Carry1 (thirtytwo\_bitsub1/Carry13)

LUT3:I1->O 3 0.479 0.941 thirtytwo\_bitsub1/fa\_14/Carry1 (thirtytwo\_bitsub1/Carry14)

LUT3:I1->O 3 0.479 0.941 thirtytwo\_bitsub1/fa\_15/Carry1 (thirtytwo\_bitsub1/Carry15)

LUT3:I1->O 3 0.479 0.941 thirtytwo\_bitsub1/fa\_16/Carry1 (thirtytwo\_bitsub1/Carry16)

LUT3:I1->O 3 0.479 0.941 thirtytwo\_bitsub1/fa\_17/Carry1 (thirtytwo\_bitsub1/Carry17)

LUT3:I1->O 3 0.479 0.941 thirtytwo\_bitsub1/fa\_18/Carry1 (thirtytwo\_bitsub1/Carry18)

LUT3:I1->O 3 0.479 0.941 thirtytwo\_bitsub1/fa\_19/Carry1 (thirtytwo\_bitsub1/Carry19)

LUT3:I1->O 3 0.479 0.941 thirtytwo\_bitsub1/fa\_20/Carry1 (thirtytwo\_bitsub1/Carry20)

LUT3:I1->O 3 0.479 0.941 thirtytwo\_bitsub1/fa\_21/Carry1 (thirtytwo\_bitsub1/Carry21)

LUT3:I1->O 3 0.479 0.941 thirtytwo\_bitsub1/fa\_22/Carry1 (thirtytwo\_bitsub1/Carry22)

LUT3:I1->O 3 0.479 0.941 thirtytwo\_bitsub1/fa\_23/Carry1 (thirtytwo\_bitsub1/Carry23)

LUT3:I1->O 3 0.479 0.941 thirtytwo\_bitsub1/fa\_24/Carry1 (thirtytwo\_bitsub1/Carry24)

LUT3:I1->O 3 0.479 0.941 thirtytwo\_bitsub1/fa\_25/Carry1 (thirtytwo\_bitsub1/Carry25)

LUT3:I1->O 3 0.479 0.941 thirtytwo\_bitsub1/fa\_26/Carry1 (thirtytwo\_bitsub1/Carry26)

LUT3:I1->O 3 0.479 0.941 thirtytwo\_bitsub1/fa\_27/Carry1 (thirtytwo\_bitsub1/Carry27)

LUT3:I1->O 3 0.479 0.941 thirtytwo\_bitsub1/fa\_28/Carry1 (thirtytwo\_bitsub1/Carry28)

LUT3:I1->O 3 0.479 0.941 thirtytwo\_bitsub1/fa\_29/Carry1 (thirtytwo\_bitsub1/Carry29)

LUT3:I1->O 3 0.479 0.830 thirtytwo\_bitsub1/fa\_30/Carry1 (thirtytwo\_bitsub1/Carry30)

LUT4:I2->O 1 0.479 0.681 thirtytwo\_bitsub1/fa\_32/Mxor\_Sum\_xo<0>11 (N01)

MUXF5:S->O 1 0.540 0.681 Mmux\_z50 (z\_31\_OBUF)

OBUF:I->O 4.909 z\_31\_OBUF (z<31>)

----------------------------------------

Total 50.138ns (20.534ns logic, 29.604ns route)

(41.0% logic, 59.0% route)

=========================================================================

Total REAL time to Xst completion: 9.00 secs

Total CPU time to Xst completion: 9.16 secs

-->

Total memory usage is 188280 kilobytes

Number of errors : 0 ( 0 filtered)

Number of warnings : 2 ( 0 filtered)

Number of infos : 0 ( 0 filtered)



